FIG. 1A
PRIOR ART

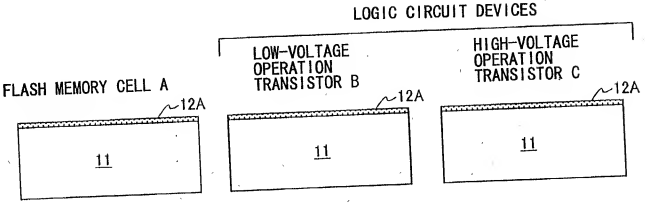


FIG. 1B
PRIOR ART

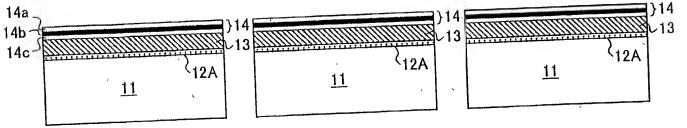


FIG. 1C
PRIOR ART

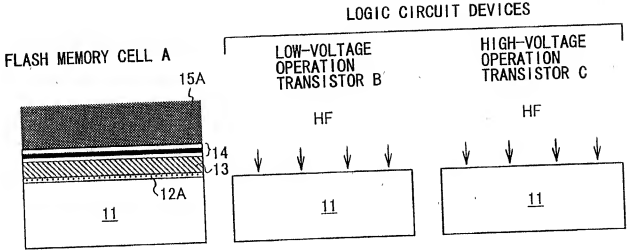


FIG. 1D
PRIOR ART

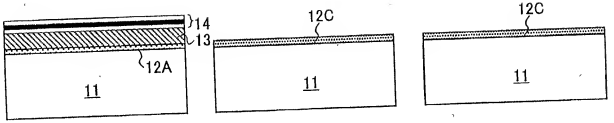


FIG. 1E
PRIOR ART

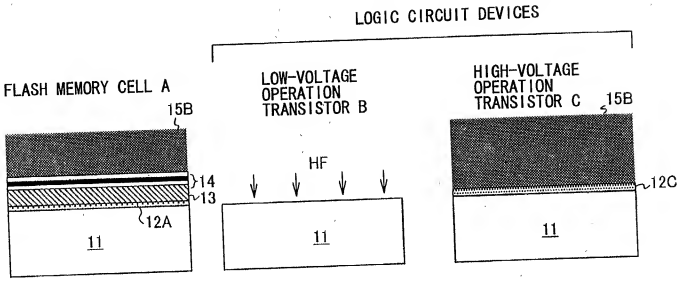


FIG. 1F
PRIOR ART

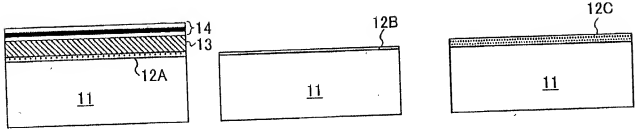


FIG. 1G
PRIOR ART

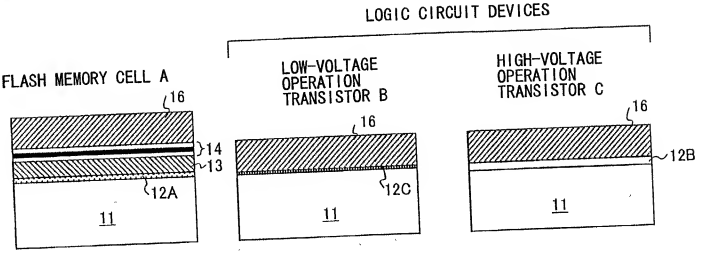


FIG. 1H
PRIOR ART

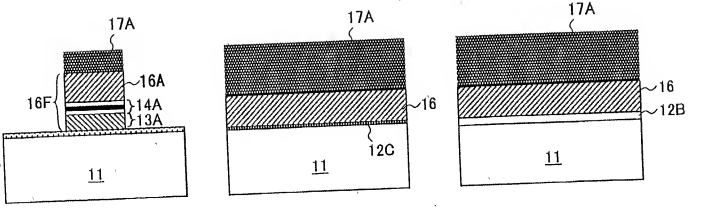


FIG. 1I
PRIOR ART

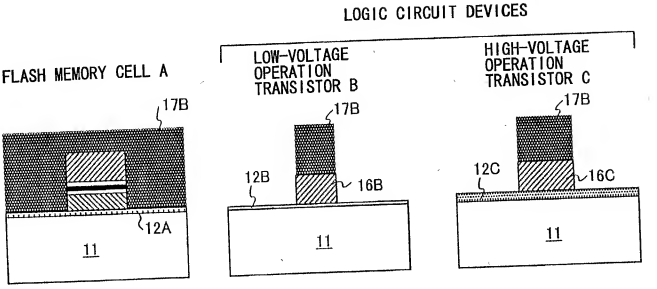


FIG. 1J
PRIOR ART

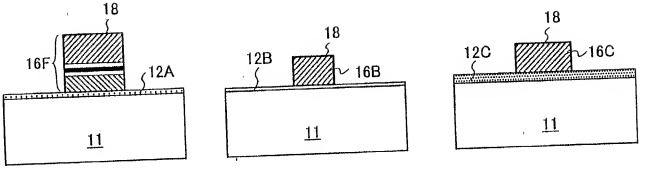


FIG. 1K
PRIOR ART

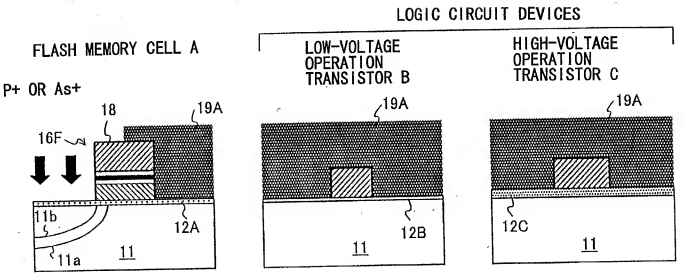


FIG. 1L
PRIOR ART

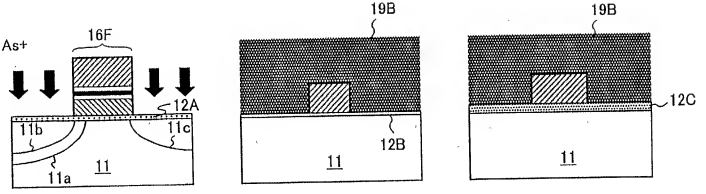


FIG. 1M
PRIOR ART

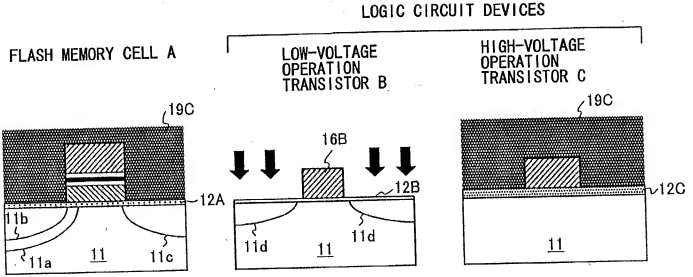


FIG. 1N
PRIOR ART

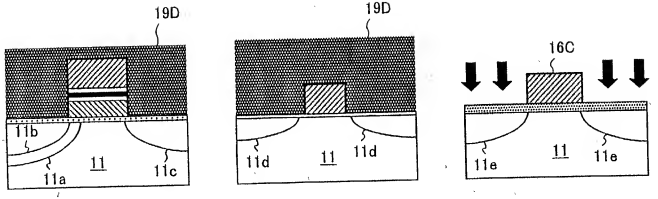


FIG. 10
PRIOR ART

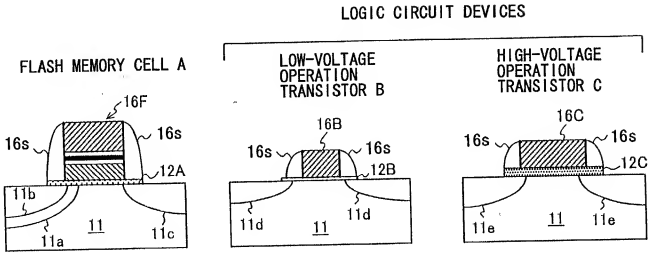


FIG. 1P
PRIOR ART

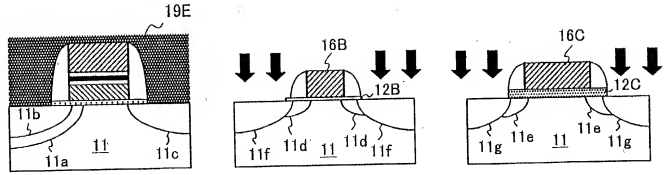
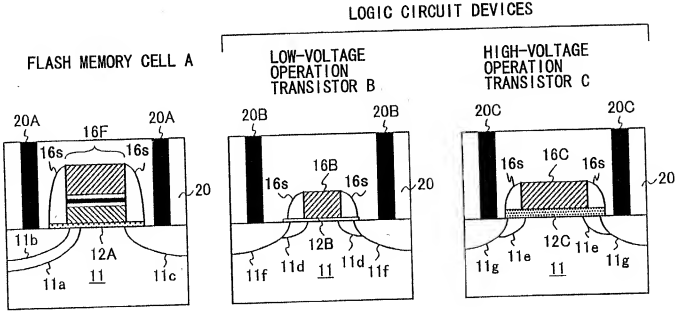


FIG. 1Q
PRIOR ART



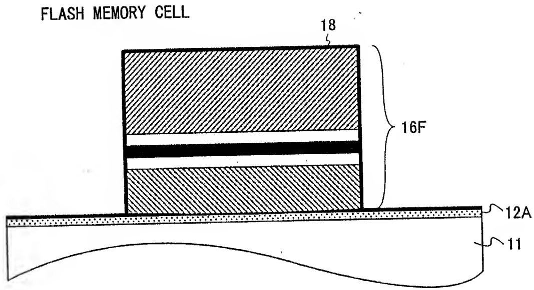


FIG. 2A
PRIOR ART

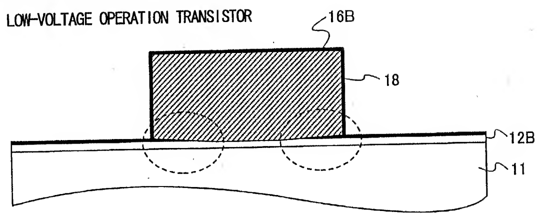


FIG. 2B
PRIOR ART

FIG. 3A
PRIOR ART

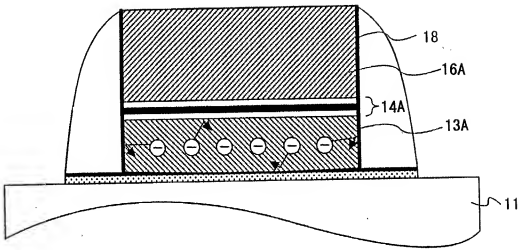


FIG. 3B
PRIOR ART

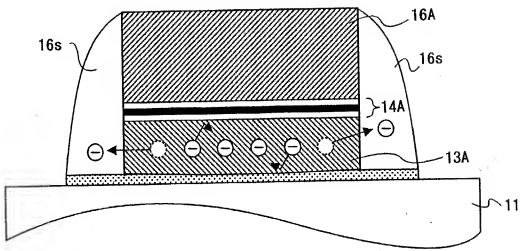


FIG. 4 RELATED ART

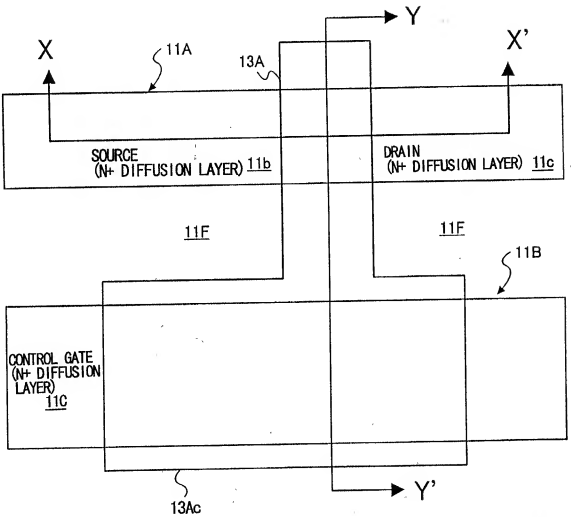


FIG. 5A
RELATED ART

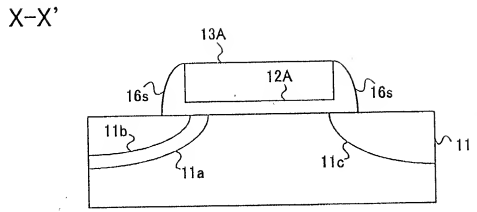


FIG. 5B
RELATED ART

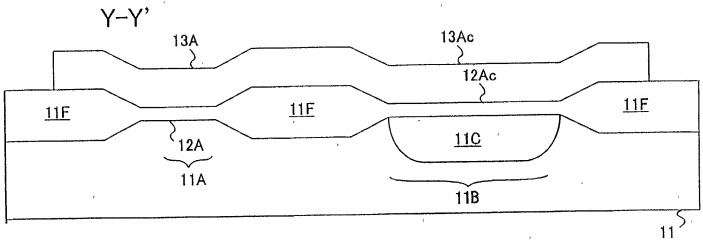


FIG. 6A
RELATED ART

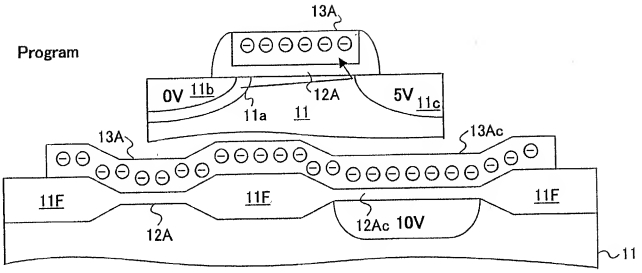


FIG. 6B
RELATED ART

FIG. 6C
RELATED ART

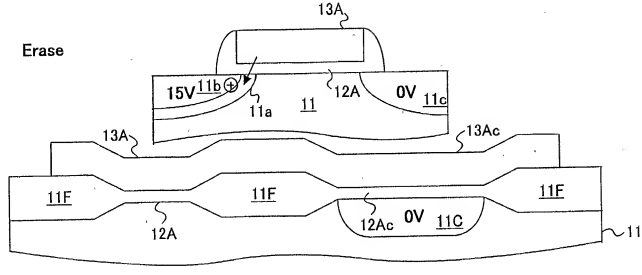


FIG. 6D
RELATED ART

FIG. 7A
RELATED ART

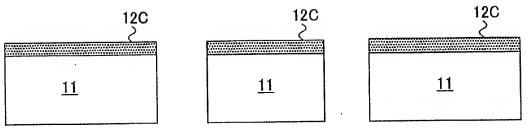


FIG. 7B
RELATED ART

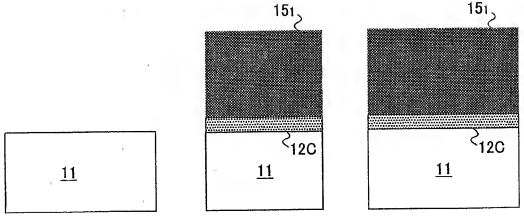


FIG. 7C
RELATED ART

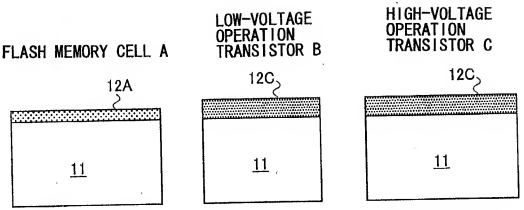


FIG. 7D
RELATED ART

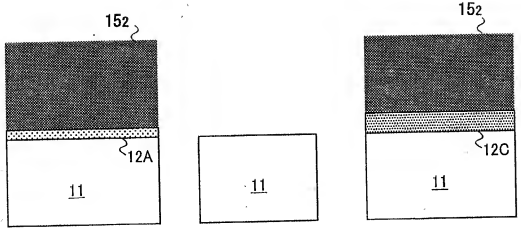


FIG. 7E
RELATED ART

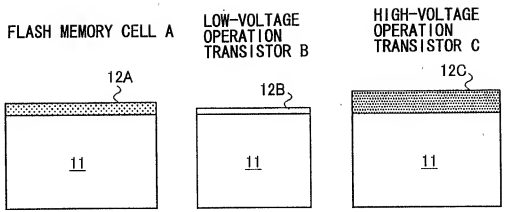


FIG. 7F
RELATED ART

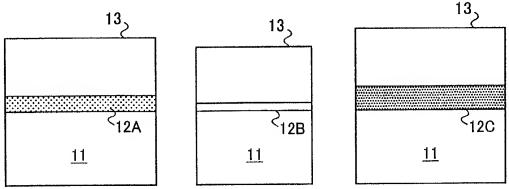


FIG. 7G
RELATED ART

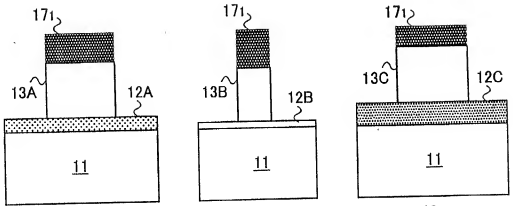


FIG. 7H
RELATED ART

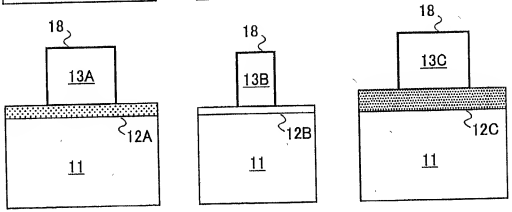


FIG. 7I
RELATED ART

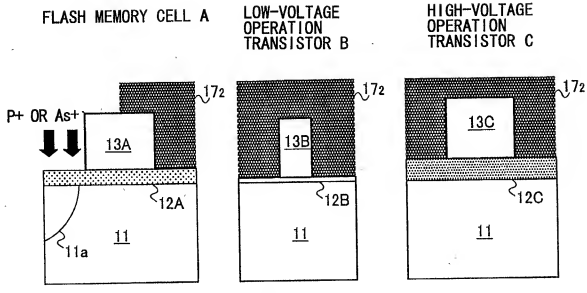


FIG. 7J
RELATED ART

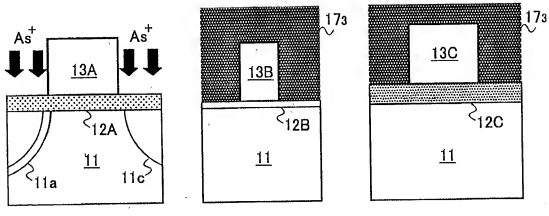


FIG. 7K
RELATED ART

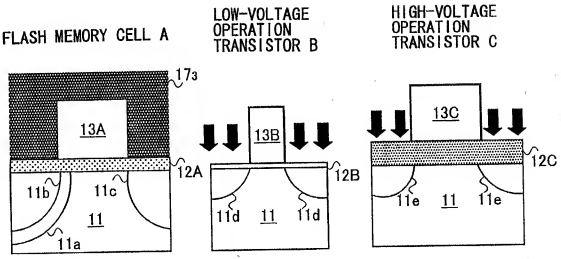


FIG. 7L
RELATED ART

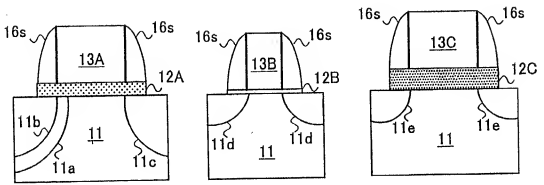


FIG. 7M
RELATED ART

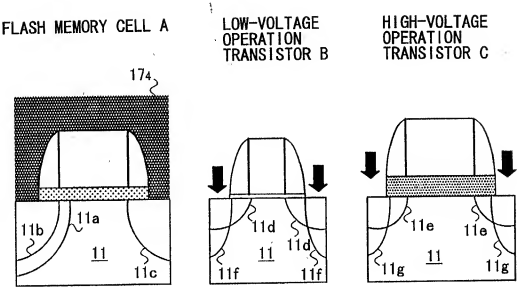


FIG. 8A
RELATED ART

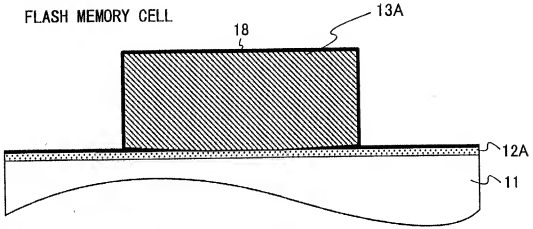


FIG. 8B
RELATED ART

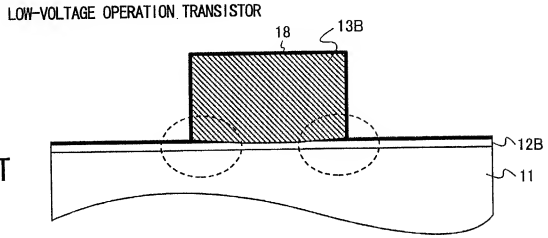


FIG. 9A

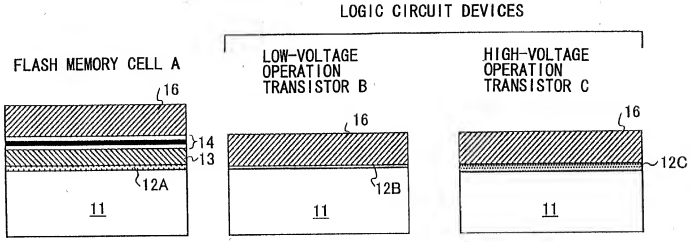

LOGIC CIRCUIT DEVICES
FLASH MEMORY CELL A
LOW-VOLTAGE OPERATION TRANSISTOR B
HIGH-VOLTAGE OPERATION TRANSISTOR C
16
14
13
12A
11
16
12B
11
16
12C
11

FIG. 9B

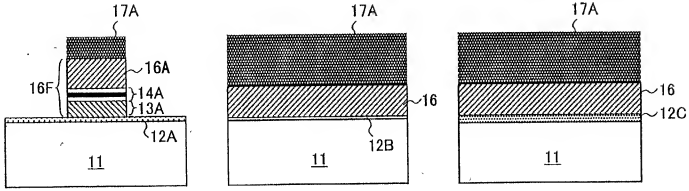

17A
16A
16F
14A
13A
12A
11
17A
16
12B
11
17A
16
12C
11

FIG. 9C

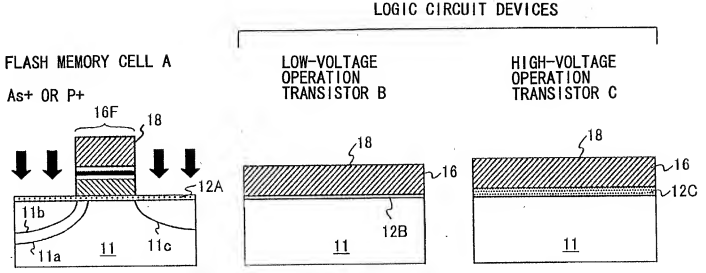

LOGIC CIRCUIT DEVICES
FLASH MEMORY CELL A
As+ OR P+
LOW-VOLTAGE OPERATION TRANSISTOR B
HIGH-VOLTAGE OPERATION TRANSISTOR C
16F
18
12A
11b
11a
11
11c
16
12B
12C

FIG. 9D

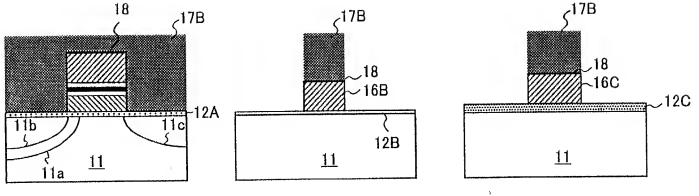

18
17B
12A
11b
11a
11
11c
16B
12B
16C
12C

FIG. 9E

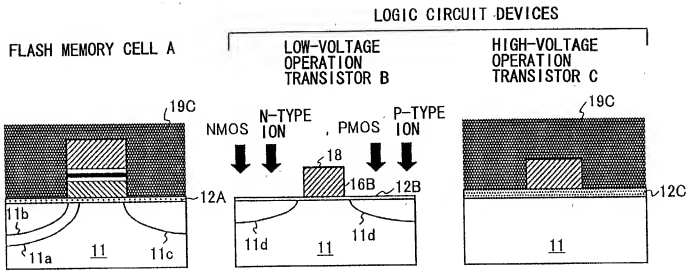

LOGIC CIRCUIT DEVICES
FLASH MEMORY CELL A
LOW-VOLTAGE OPERATION TRANSISTOR B
HIGH-VOLTAGE OPERATION TRANSISTOR C
19C
NMOS N-TYPE ION
PMOS P-TYPE ION
18
16B
12A
12B
12C
11b
11a
11
11c
11d
11d
11
11
19C
19C
12C

FIG. 9F

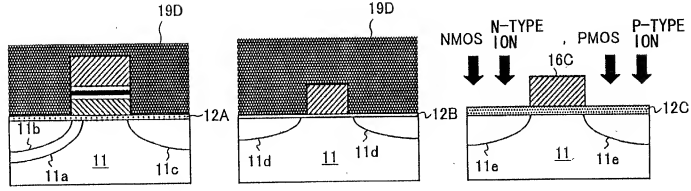

19D
19D
NMOS N-TYPE ION
PMOS P-TYPE ION
16C
12A
12B
12C
11b
11a
11
11c
11d
11
11d
11e
11
11e

FIG. 9G

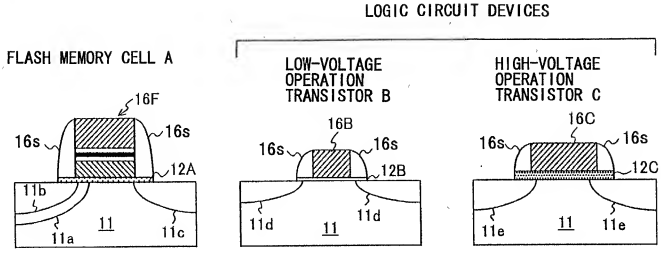

FLASH MEMORY CELL A
LOGIC CIRCUIT DEVICES
LOW-VOLTAGE OPERATION TRANSISTOR B
HIGH-VOLTAGE OPERATION TRANSISTOR C
16F
16s
16s
12A
11b
11a
11
11c
16B
16s
16s
12B
11d
11
11d
16C
16s
16s
12C
11e
11
11e

FIG. 9H

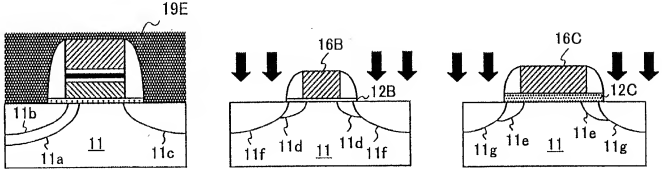

19E
11b
11a
11
11c
16B
12B
11f
11d
11
11d
11f
16C
12C
11g
11e
11
11e
11g

FIG. 91

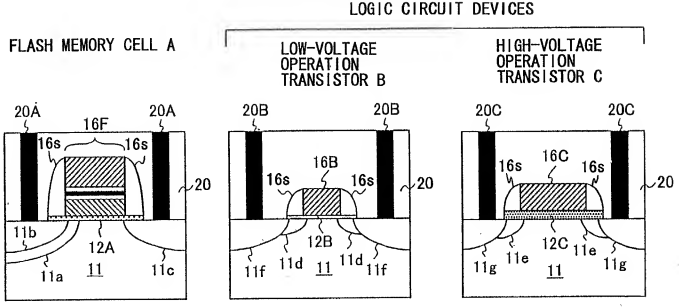

LOGIC CIRCUIT DEVICES
FLASH MEMORY CELL A
LOW-VOLTAGE OPERATION TRANSISTOR B
HIGH-VOLTAGE OPERATION TRANSISTOR C
20A
16F
16s
16s
20A
20
11b
12A
11a
11
11c
20B
20B
16B
16s
16s
20
12B
11f
11d
11
11d
11f
20C
20C
16C
16s
16s
20
12C
11e
11g
11
11e
11g

FIG. 10A

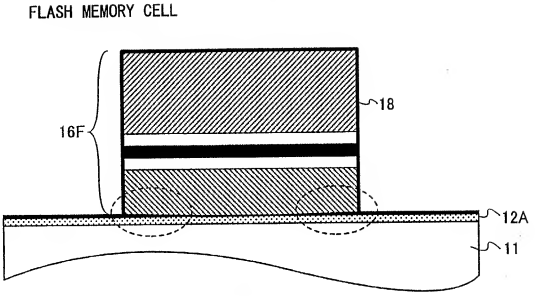


FIG. 10B

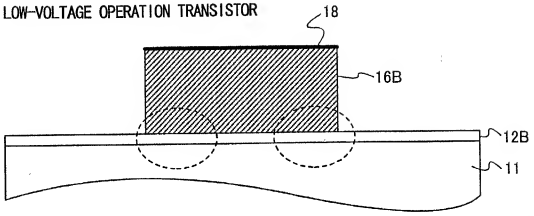


FIG. 11A

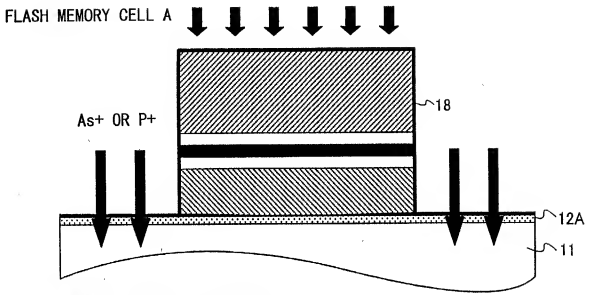


FIG. 11B

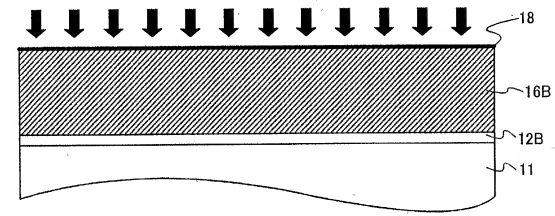


FIG. 12A

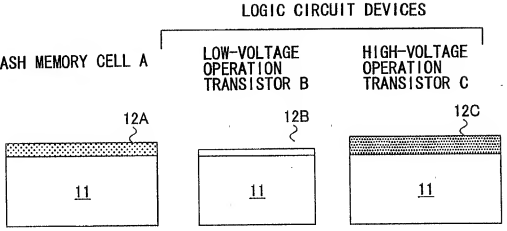


FIG. 12B

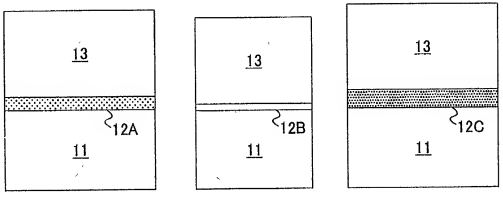


FIG. 12C

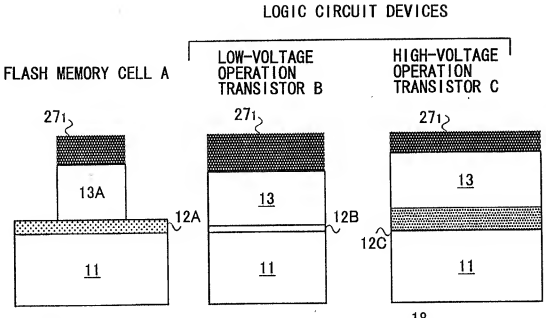


FIG. 12D

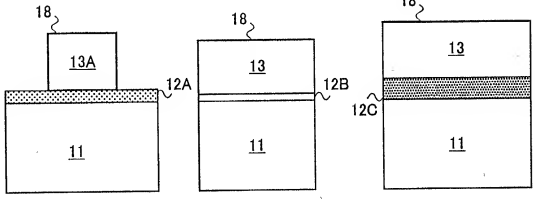


FIG. 12E

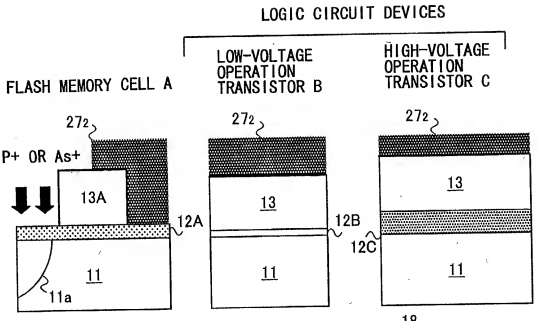


FIG. 12F

FIG. 12G

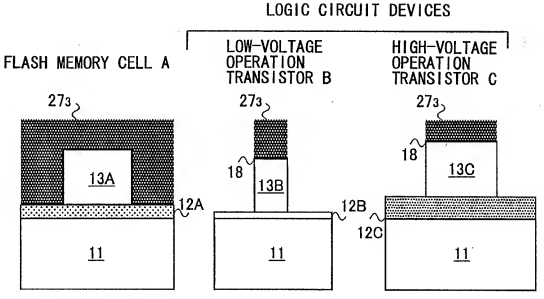


FIG. 12H

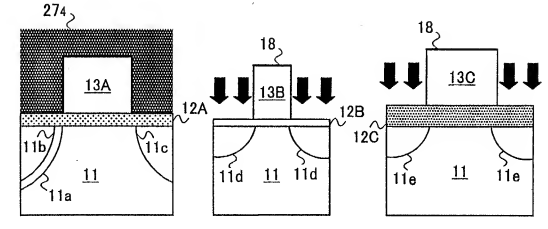


FIG. 121

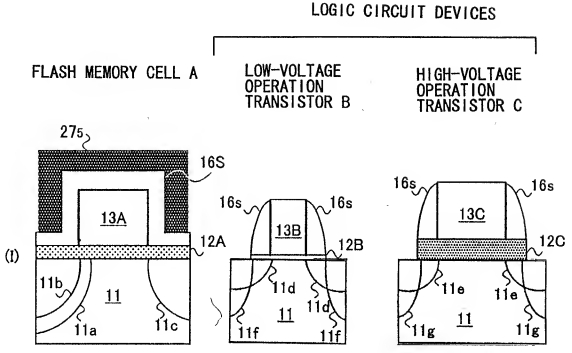

LOGIC CIRCUIT DEVICES
FLASH MEMORY CELL A
LOW-VOLTAGE OPERATION TRANSISTOR B
HIGH-VOLTAGE OPERATION TRANSISTOR C
(I)
27s
16S
13A
12A
11b
11
11a
11c
16s
16s
13B
12B
11d
11d
11
11f
11f
16s
16s
13C
12C
11e
11e
11g
11
11g

FIG. 13A

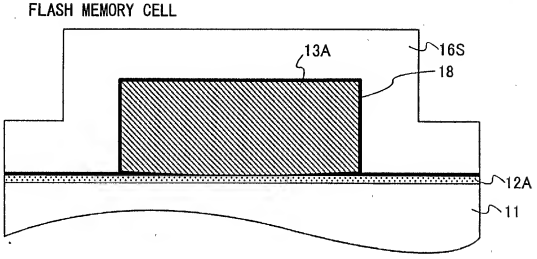


FIG. 13B